

Call for Papers

Austrochip is an annual workshop on microelectronics and integrated circuits in Austria and neighboring countries. The 24th edition will be organized by the Integrated Systems and Circuits Design Group of Carinthia University of Applied Sciences in Villach.

Topics of the workshop include but are not limited to:

- Analog, mixed-signal, and RF integrated circuits
- Digital circuits, filters, DSPs, asynchronous designs
- FPGA design and reconfigurable hardware
- Design methodology, system-level design, gigascale circuits, network-on-chip
- Embedded systems, low-power designs, RF systems, security aspects
- Verification and testing, signal integrity, device modelling, timing analysis, reliability simulation
- Emerging technologies, nano CMOS process, sub-threshold circuits, sensors, organic and biomedical electronics
- Case studies and prototyping

Submissions from academia as well as industry are welcome. Especially, PhD-Students are invited to present their research work related to topics of Austrochip, but also excellent MSc-Theses will be considered.

Submissions will be double-blind-reviewed. Accepted papers will be made available electronically at the conference (USB-stick) and we plan to publish all papers written in English through IEEE Xplore (with indexing by well-known major indexing services).

Instructions for Authors:

Papers should not exceed 6 pages IEEE format (including bibliography and appendix). Instructions and additional details can be found at <http://austrochip.fh-kaernten.at/submission>

Conference Venue:

Austrochip 2016 is held in Villach on October 19th, 2016 at the Holiday Inn Hotel. Registered participants will be provided with proceedings USB stick, lunch and coffee breaks.

Contact/Organization:

Manfred Ley, Carinthia University of Applied Sciences - ISCD

Email: [austrochip\(at\)fh-kaernten.at](mailto:austrochip(at)fh-kaernten.at)

Web: <http://austrochip.fh-kaernten.at/>

Conference Venue



Important Dates

Submission Deadline
July 10th, 2016 extended
~~June 27th, 2016~~

Acceptance Notification
August 30th, 2016

Workshop
October 19th, 2016

Organizer



[ISCD – Integrated Systems
and Circuits Design](#)

Technical co-sponsors



Technical Program Committee:

Mario Auer	Graz University of Technology (IFE)
Thomas Bauernfeind	Intel Mobile Communications Austria
Bernd Deutschmann	Graz University of Technology (IFE)
Dieter Draxelmayr	Infineon Technologies Austria
Michael Gebhart	NXP Semiconductors Austria
Gerald Hilber	Johannes Kepler University of Linz (RIIC)
Rainer Holzhaider	ams AG
Martin Horauer	University of Applied Sciences Technikum Vienna (ES)
Mario Huemer	Johannes Kepler University of Linz (ISP)
Nikolaus Kerö	Oregano Systems
Hans-Peter Kreuter	Infineon Technologies Austria
Jakob Lechner	RUAG SPACE GmbH
Manfred Ley	Carinthia University of Applied Sciences, Villach (ISCD)
Wolfgang Mayerwieser	Dialog Semiconductor
Christian Netzberger	FH Joanneum, University of Applied Sciences, Kapfenberg
Erwin Ofner	Carinthia University of Applied Sciences, Villach (ISCD)
Timm Ostermann	Johannes Kepler University of Linz (RIIC)
Thomas Polzer	Vienna University of Technology (ECS)
Karl-Christian Posch	Graz University of Technology (IAIK)
Peter Rössler	University of Applied Sciences Technikum Vienna (ES)
Kerstin Schneider-Hornstein	Vienna University of Technology (EMCE)
Peter Söser	Graz University of Technology (IFE)
Andreas Steininger	Vienna University of Technology (ECS)
Johannes Sturm	Carinthia University of Applied Sciences, Villach (ISCD)
Gunter Winkler	Graz University of Technology (IFE)
Johannes Wolkerstorfer	xFace, Graz
Horst Zimmermann	Vienna University of Technology (EMCE)

Patrons

